Technology Overview

SiliconIntervention Technology for Low Noise Signal Processing

Overview

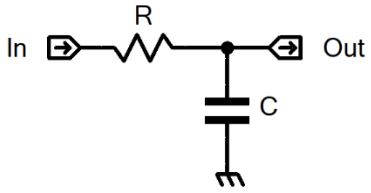
Low noise in a signal processing device requires low value resistors and high currents due to basic thermodynamic limitations. Inefficiencies exist when DC currents need to flow through these low value resistors, for example in the single to differential convertor of a balance output Audio DAC. Such inefficiencies can be removed with equal common mode voltage differential signal processing, but this note goes one step further and proposes to process signals as charges on capacitors which, if unswitched, exhibit exactly no thermal noise. This is a means to achieve the lowest possible current consumption in high performance signal processing.

Introduction

Is kT/C noise fundamental in the same way that thermal noise in a resistor is fundamental? The answer is yes, with certain assumptions.

kT/C noise is a convenient and simple result of the analysis of the noise that will be sampled onto a capacitor when a switch connects that capacitor to a signal source. The analysis proceeds as follows.

The noise of this circuit is generated by the resistor since the charge flowing in the resistor is in thermal equilibrium with the environment[1].



The noise generated by the resistor represents an energy per unit bandwidth of 4kT from thermodynamic principles[2], as is well-known, consequently a noise voltage of $\sqrt{4kTR}$ is present per unit bandwidth into the capacitor.

The total noise present is the integral of this noise voltage weighted by the noise bandwidth of the filter created by the RC.

The noise bandwidth of a single RC filter is the value of $\int_0^\infty \frac{1}{1+\left(\frac{w}{wc}\right)^2}$, which is $\frac{\pi}{2} \cdot \omega c$ where $\omega c = \frac{1}{2\pi RC}$; hence the total noise variance is $\frac{4kTR.\pi}{4\pi RC}$ most of which cancels to leave kT/C.

We see that the resistance R cancels in the total noise expression, hence R can be arbitrarily large and the resulting sample-and-hold action $R \to \infty$ has captured a noise voltage of $\sqrt{kT/C}$.

Thus, any switching action capturing a signal onto a capacitor[3] exhibits a noise variance kT/C – which is the common "rule of thumb".

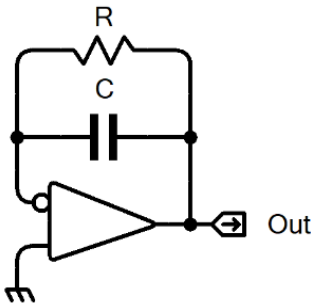
[1] Contrast this to the charge stored on a capacitor: that charge is *not* in thermal equilibrium since there is no means for the charge to escape the capacitor and come into equilibrium with the environment. The charge on a capacitor is not in thermal equilibrium with the environment and no fluctuation of voltage is present. This is the basis of a battery: thermal equilibrium of a charge storage device begins only when the charge can escape the capacitive element.

[2] The '4' in the equation arises from the presumption that two equal resistors in series may represent the thermal connection between the example resistor and a second representing the thermal environment. Thus, the energy dissipated in the pair is V^2/2R, half of which is the example resistor V^2/4R and this is kT, hence 4kTR voltage variance per unit bandwidth.

[3] We now see further qualifications: that the noise bandwidth be defined by the capacitor onto which the sample is taken (which is not always the case) and that the noise is always present in the bandwidth defined by the RC in the absence of any change in the R value, that is, in the absence of any sampling action.

Signal Processing without kT/C Noise

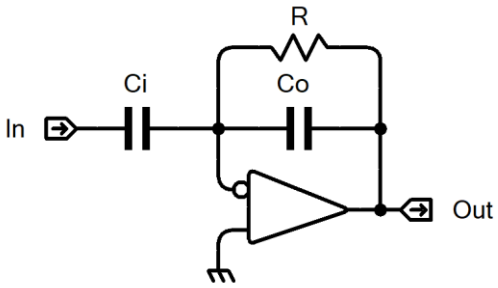
Assuming the op-amp is perfect, the noise of this



circuit can immediately be seen to be kT/C: the noise is originating in the resistor and is applied to a first order filter defined by RC.

However, because that noise is the integral noise in the bandwidth defined by the RC time constant ($1/2\pi RC$) it seems reasonable to ask if we may operate *above* this bandwidth where the kT/C noise has been suppressed, in a region *where there is no kT/C noise*.

Generally, yes, we can if we do this:



The gain from input to output is Ci/Co and the bandwidth is limited by that of the amplifier. The capacitors are making no noise at all, the noise from the R is filtered by a single pole at $1/2\pi RC$, and if R is sufficiently large the kT/C noise is *below* the bandwidth of interest.

This begs two questions: firstly, why have the resistor at all? Remove that component and there is no noise (assuming the op-amp is perfect).

In fact, it is not possible to remove the resistor, or the DC condition is unknown. It is always necessary to define the DC condition in capacitor coupled circuits and while the voltages on Ci are defined (In and Ground respectively) the voltage on Co is undefined without some resistance R connected as shown which results in no gain, a defined voltage, at frequencies approaching zero.

Secondly, this seems so trivial why has it not been done before?

The answer is that it is impractical. Consider the audio application with a bandwidth of interest from 20hz to 20kHz. Assuming that the Co value is 100pF (which is quite large to place on a silicon chip) the R value must be such that $20 \gg 1/2\pi RC$, or $R \gg \frac{1e10}{40\pi} or \gg 80M\Omega$ which is generally not possible on a silicon chip.

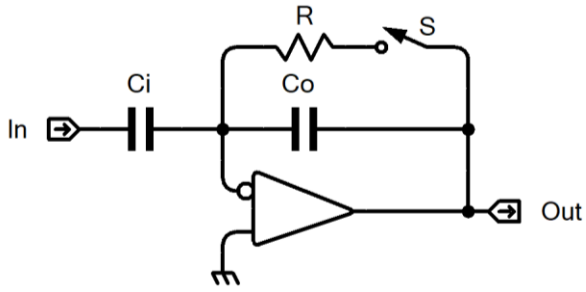
The problem of moving the kT/C noise to below the band of interest corresponds to defining a high pass filter, with on-chip components, that is at a very low frequency, and this requires very high value resistors which are impractical.

Solutions to the High Resistor value

Time division multiplexed (TDM) resistor

One means that springs to mind is that used in a phase-locked loop (PLL): in PLL designs a similar need arises to define a capacitor voltage with a very long time constant. In PLL designs the phrase “charge pump” is used since this best describes what is occurring in the circuit: a time division multiplexed (TDM) feedback is applied to nudge up or nudge down the voltage on a capacitor.

It may seem that this circuit utilizing a TDM resistor, should work, and in certain circumstances it does indeed work:



The switch S is activated with a low duty cycle, say 1% of the time it is closed, so making the R value appear to be 100x larger.

We know from the analysis on page one that the noise is still kT/C, and we can see that there is a sampling action at the rate of operation of the switch. Consequently, a new value of noise is sampled onto the output signal at the switching rate. It is a square wave signal with arbitrarily low frequency components, so once again if that switching frequency were lower than the signal of interest (lower than 20hz in the Audio example) this may be a viable solution if pop noise may be ignored.

In the TDM resistor solution discussed here there will be a constant sequence of "pops" as the resistor samples the kT/C noise. 100pF will induce a pop noise of 6.4µV per change and this is too high to be ignored.

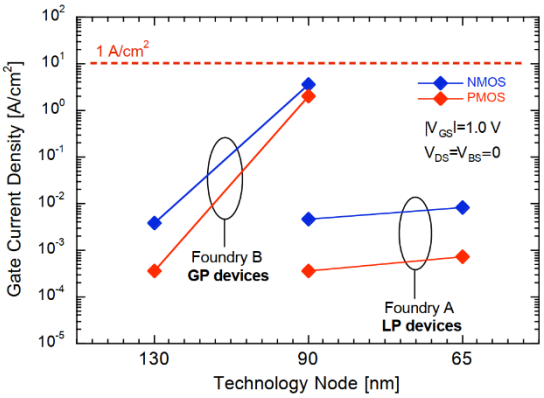
In addition to the problem of pop noise our proposed TDM resistor must provide any gate current (input current) that the op-amp requires.

As explained in the following section, the need to provide a finite gate current into the op-amp rules out any solution involving a high value resistor (TDM or otherwise) because the voltage required to drive the gate current is many tens of volts – far higher than the circuit can provide.

Tunneling Current replaces high value resistor

In advanced CMOS processes the input devices of the op-amp have thin gate oxides and a non-negligible gate current.

Gate current flows because carriers can tunnel across the insulating barrier due to quantum mechanical effects present at such low gate thicknesses.



The gate current is proportional to the gate area, larger area creating more gate current. 1/F noise, which is a limiting factor in many applications, is inversely proportional to gate area. Consequently, to lower the 1/F noise the gate area is large, giving rise to a large and far from negligible gate current.

The gate current for a PMOS device of large area may be estimated by simulation, but some guidance may be inferred from the above drawing [4].

This indicates we may expect 100A/sq meter (10mA per sq cm on the graph – "Foundry A LP devices") of gate area for the 65nm process.

Typical PMOS for low 1/F noise may have a gate area of more than 2n sqm (for example, 16u by 2u by 64 is 2.048n sqm) implying a potential gate current of 200nA or more. This gate current must be provided by the resistor in our circuit which is large. For example, if an op-amp gate current of 200nA is present with a 100MΩ resistor, a voltage of 20V would be required.

Gate current represents a loss of power for low power digital signal processing, and consequently manufacturers often offer a Low-

[4] https://indico.cern.ch/event/190941/contributions/1466437/attachments/271602/380058/traversi.pdf (However note this error in this figure: the author has mistaken the 10A y-axis for the 1A value – according to this figure, Foundry B GP devices are exceeding 1A per square centimeter, contrary to the text of the document.)

Power varient of their processes. Data from the TSMC 65nm process shows the following gate currents. The sizes are 16u x 2u x 64 (W, L, M) for each device with 50µA drain current:

65nm	Current GP (nA)	Current LP (nA)
NMOS	58	0.28
PMOS	204	0.24

Gate current in the low power variant (LP) of the process is much lower than in the standard (GP) version. From a DC bias point of view the LP version of the process is necessary since otherwise the gate current cannot be provided through the very high resistor needed to cause the kT/C noise to be below the band of interest.

A further result from the Global Foundary 22nm FDX process shows these results. The FETS are 2u x 125n x 8000 (W, L, M). The thin oxide devices (SG as described by Global) are lvtnfet and lvtpfet having 1.25nm and 1.45nm oxide thickness respectively. The EG variant of the devices, eglvnfet and eglvpfet, have 3.4nm and 3.65nm gate oxides respectively.

22nm	Current SG (nA)	Current EG (nA)
NMOS	~1,000	0.01
PMOS	>10,000	<0.3

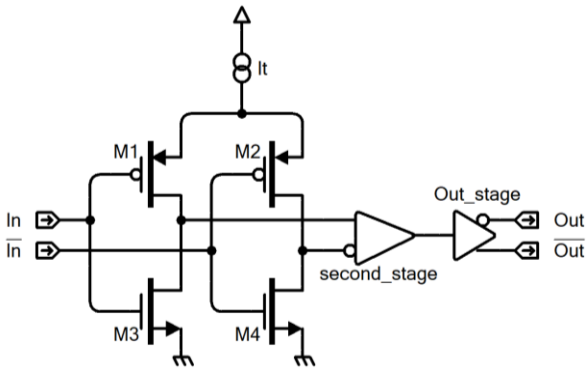
The EG variant of the process shows much lower gate current leakage, (but unlike in the TSMC 65nm process it may *not* be possible to balance the NMOS against the PMOS current since they are of such different magnitudes).

Circuits Using Quantum Gate Tunneling

An Alternate Amplifier Configuration

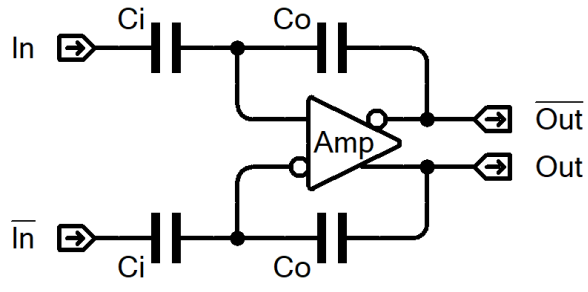
If we build the input stage of an amplifier in an unconventional way we can achieve a lower noise and we can solve the problem that the kT/C noise cancellation (removal of kT/C noise to below the band of interest) requires a large value resistor. This is possible due to the capacitively coupled signal path.

Specifically, the op-amp follows this topology[5]:



There is no common mode range on this amplifier (we do not need any CMR if the circuit is using capacitors in the processing path). The input voltages are such that the NMOS M3 and M4 each carry half the tail current, It. The PMOS devices M1 and M2 also participate in the input transconductance, there is no current source or mirror load for the NMOS devices, rather there is a second input pair, the PMOS, working into the same second stage[6].

The intention is that this form of amplifier be connected to the capacitively coupled circuit in a fully differential configuration:



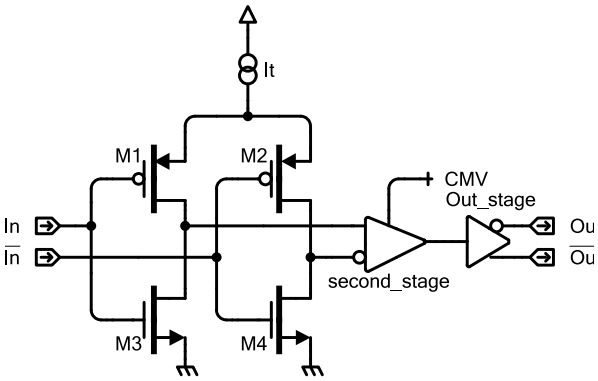
[5] More details of which may be found here: https://patentscope.wipo.int/search/en/detail.jsf?docId=WO2011069231

[6] This three-stage amplifier will consequently have 3db better noise (for any given current 'It') than any possible load that could be connected to the NMOS pair: even a perfect load network has half the Gm of this quad input configuration. Furthermore, the 1/F noise is that due to the sum of the areas of the NMOS and PMOS and hence is also 3db lower.

The differential circuit above has a gain of Ci/Co, the fixed common mode is not an issue since the input nodes are purely capacitively coupled. But the configuration has no defined DC bias and cannot provide any finite op-amp input current.

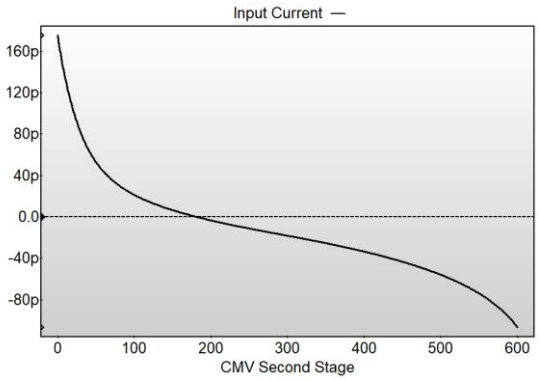
A modification to the amplifier topology can solve this problem as follows.

The common mode input voltage of the second stage is a 'free variable' and may be made adjustable.



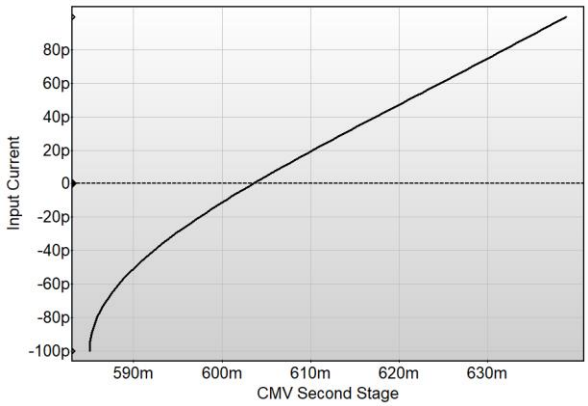
This has no effect on the basic circuit operation since there is a range[7] of acceptable output common mode voltages of the first stage.

However, this adjustable second stage common mode voltage controls the tunneling current of the input devices:



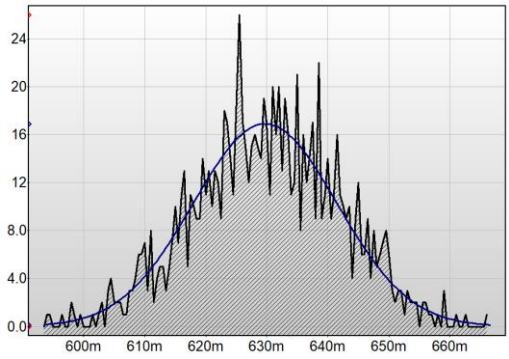
As the Drain-Source voltage of the input FETS are changed, either the PMOS gate tunneling current or the NMOS gate tunneling current dominates.

Here is shown the detail of the circuit's ability to compensate for a small current injected into the input on the TSMC 65nm process[8]:



Note that the current change at the input is approximately 3nA/V or 330MΩ.

This is the Monte-Carlo analysis with process and local variations modelled:



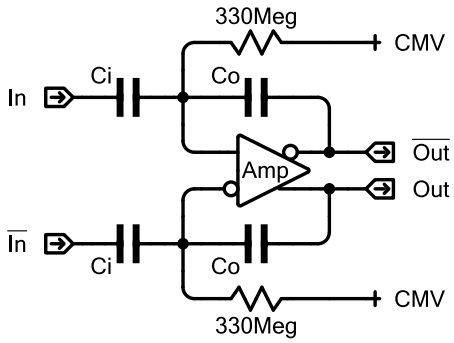
The phenomenon is robust in the presence of process variations.

[7] The allowed input CMV to the second stage where the amplifier will still work extends from approximately $V_{gs}^N - V_{th}^N$ up to $V_{gs}^N + V_{th}^P$

[8] This is a design now optimized for tunneling current control. The relative sizes of the NMOS and PMOS are adjusted to give about 600mV for zero input current

Equivalent Circuit

With this feature in place we may model the capacitor coupled amplifier as shown here:



The large resistor indicates the equivalent tunneling current control – there is no actual resistor in the circuit[9].

We may connect the CMV control to the output which will create a high pass filter. Assuming Co is ~30pF, the kT/C noise is now limited to less than 20Hz. There is no kT/C noise present in signal bands above 20Hz. This can be exploited to greatly reduce power and chip area.

Tunneling Current has Noise

The circuit is operating by balancing the quantum tunneling current of the PMOS against the NMOS. This will root-sum-square the noise present in the individual tunneling currents and a noise like 1/F noise (rising with decreasing frequency) will result[10].

In a practical design there is a trade-off between the 1/F noise from the FETS and the 1/F-like noise from the tunneling current itself. As the FET areas are increased 1/F noise from the FETS decreases, 1/F-like noise from tunneling current increases. There is therefore an optimum input device size. Our designs use this optimum point.

Advantage in a Typical Application: Audio

Using high performance Audio as an example: in a 1V RMS system with 4nV/√Hz noise at least one 1kΩ resistor will have more than 1V across it and hence this resistor alone consumes 1mA. This is the current flow needed to create the voltage excursion across the low noise components of the audio system.

Using the quantum tunneling circuit described here, a typical capacitor value of 30pF may be used (to remove all kT/C noise from the band). At 20kHz that capacitor consumes less than 4µA. This is 250x lower current needed to create the voltage excursion. All the available current may be directed to lowering the noise of the op-amps themselves.

The quantum tunneling current signal to noise ratio is limited only by the noise from the amplifier and has the potential to consume significantly lower power.

Use in ADC and DAC systems

The circuit need not be a simple amplifier: the same input stage and tunneling control can be applied in a ΣΔ ADC where the input and feedback elements are entirely capacitive. This results in a >108dB ADC consuming ~100µA. (The same design consumes ~5µA total if 80db SNR is sufficient for the application)

A complete Audio DAC >108dB using this technique consumes ~200µA.

Conclusion

Using this method, unswitched capacitors that generate no noise can be the elements in the analog signal path. There will always be noise from other elements that are maintaining the DC operating point, but that noise is below the band of interest. Consequently, the lowest current for any given noise specification is achieved with this technique.

Martin Mallinson, SI Inc.

[9] Consequently, there is no problem of input current flowing through resistors, no high voltage is required.

[10] Because of the integration action of this charge onto the feedback capacitor.